Fast Packet processing in VNF using DPDK and fd.io

Abstract

Packet processing in the fast path involves looking up bit patterns and deciding on an actions at line rate. The complexity of these functions at Line Rate, have been traditionally handled by ASICs and NPUs. However with the availability of faster and cheaper CPUs and hardware/software accelerations, it is possible to move these functions onto commodity hardware. This tutorial will talk about the various building blocks available to speed up packet processing both hardware based e.g. SR-IOV, RDT, QAT, VMDq, VTD and software based e.g. DPDK, Fd.io/VPP, OVS etc and give hands on lab experience on DPDK and fd.io fast path look up with following sessions. 1: Introduction to Building blocks: Sujata Tibrewala 2: DPDK HASH Library Hands-on training: Saikrishna Edupuganti 3: DPDK IP Pipeline Hands-on: Muthurajan Jayakumar 4: FD.io VPP Architecture and Hands-on Training: Ray Kinsella

Audience

The audience is anyone working in network software development, specially those who are interested in understanding various building blocks in SDN/NFV and how to move the standard Network functions onto a virtualized environment.

Experience Level

Intermediate

Benefits to the Ecosystem

It will help the eco system understand how to use the building blocks such as Data Plane Packet Processing and FD.io along with hardware accelerators such as SR-IOV , QAT etc in order to tap into the power of standard high volume servers available in the market today.

The planned format of the workshop

Introduction followed by hands on lab exercises on remote systems

Previous submission of workshop

http://nfvsdn2016.ieee-nfvsdn.org/files/2016/09/IntelTutorial-nfv-sdn.pdf

Publicity and advertising plan to attract attendees

Send out information to all 200+ Intel Network Builders' ecosystem members
https://networkbuilders.intel.com/ecosystem

SDN and NFV Platform Ingredients and High Speed Packet Processing: Sujata Tibrewala, Network Technology Evangelist at Intel: (1 hr)

Packet processing in the fast path involves looking up bit patterns and deciding on an action based on the bit patterns present at line rate. The complexity of these functions at Line Rate, have been traditionally handled by ASICs and NPUs in most production network systems. However with the availability of faster and cheaper CPUs and hardware/software accelerations, it is possible to move these functions onto commodity hardware. This tutorial will talk about the various building blocks available to speed up packet processing both hardware based e.g. SR-IOV, RDT, QAT, VMDq, VTD and software based e.g. DPDK, Fd.io/VPP, OVS etc and give hands on lab experience on DPDK and fd.io fast path look up.

DPDK HASH Library Hands-on training: Saikrishna Edupuganti, Researcher at Intel Labs (2 hrs)

DPDK Hash library provides hashing functions and hash table data-structures. DPDK hash table has high occupancy and performance, scaling to millions of entries. It's most common application in networking is for flow classification. In this session we will get familiar with APIs and extend an example app to filter packets based on IP. Later we will deep-dive into the library internals and finally, edit library code to observe the effects on table occupancy.

DPDK IP Pipeline Hands-on: Muthurajan Jayakumar Technical Marketing Engineer at Intel Corp (2 hrs)

DPDK Internet Protocol (IP) Pipeline application is intended to be a vehicle for rapid development of packet processing applications running on multi-core CPUs. DPDK IP Pipeline provides a library of reusable functional blocks called pipelines. These pipelines can be seen as prefabricated blocks that can be instantiated and inter-connected through packet queues to create complete applications (super-pipelines).

In this session, you will build virtual Provider Edge router (vPE) in industry use case key configurations. You will partition the cores between control plane and data plane functionalities. With the ease of using lego blocks, you will connect the data plane cores in configurations ranging from run to completion to pipeline architectures.

In 4 to 5 mini-exercises, you will configure the characteristics of virtual Provider Edge router's individual pipeline stages such as 1) firewall, 2) flow classifier, 3) router and 4) Quality Of Service by creating/updating tables specific to each stage.

FD.io VPP Architecture and Hands-on Training: Ray Kinsella, Network Software Solutions Architect , Intel (2hrs)

FD.io VPP is an extensible framework that provides out-of-the-box production quality switch/router functionality. FD.io VPP is a high performance, proven technology, with modular design and flexibility, and a rich feature set. VPP is an extensible framework allowing anyone to "plug in" new graph nodes without the need to change core dataplane code. VPP technology is based on a proven technology that has shipped in Cisco products for a number of years. It now forms a cornerstone technology of the FD.io

open source community. Fd.io is an open and welcoming community for those interested in collaborating on software defined dataplane technologies.

1. Configure VPP as Container Bridge.
2. Run VPP L3 in a Container and test with ICMP.
3. Configure and extend VPP VXLAN.

Speaker Bio

Sujata Tibrewala is a Networking Community Manager and Developer Evangelist at Intel. She has a bachelors in Mathematics from IIT KGP and Masters from IISC in EE Bangalore. Her Masters work was in Stereo Vision. She started her career writing Layer2/Layer 3 code for Agere network processors. Subsequently she has worked on 802.1x security technologies at CISCO and also implemented Openflow 1.3 on CISCO switches. She also has worked with Virtualization using VMware stack, and works today on Intel assist open source technologies for SDN/NFV, and drives adoption of these technologies among developers.

M Jay has worked with the DPDK team from 2009 onwards. M Jay joined Intel in 1991 and has been in various roles and divisions with Intel – 64 bit CPU front side bus architect, 64 bit HAL developer to mention a few before DPDK team. M Jay holds 21 US Patents, both individually and jointly, all issued while working in Intel. M Jay was awarded the Intel Achievement Award in 2016, Intel's highest honor based on innovation and results.

Saikrishna Edupuganti is a researcher at Intel labs and has worked on projects such as BESS – performance benchmarking and integration effort into CORD, Scalable Switch Route Forward – a successor to RouteBricks , Integrated GPU for NFV – exploring use of iGPU for layer2-4 workloads. He works today with Intel labs involves designing solutions and working on POC and deployments with Intel’s customers and academia.

Ray Kinsella has been an active contributor to Open Source software since 1996. He is a technologist with 17 years of industry experience in Software Engineering, his particular focuses are comms, networking and virtualization, in particular Network Function Virtualization. He holds a masters in Advanced Software Engineering from University College Dublin and has 3 patents at the US Patent Office.